

Figure 1

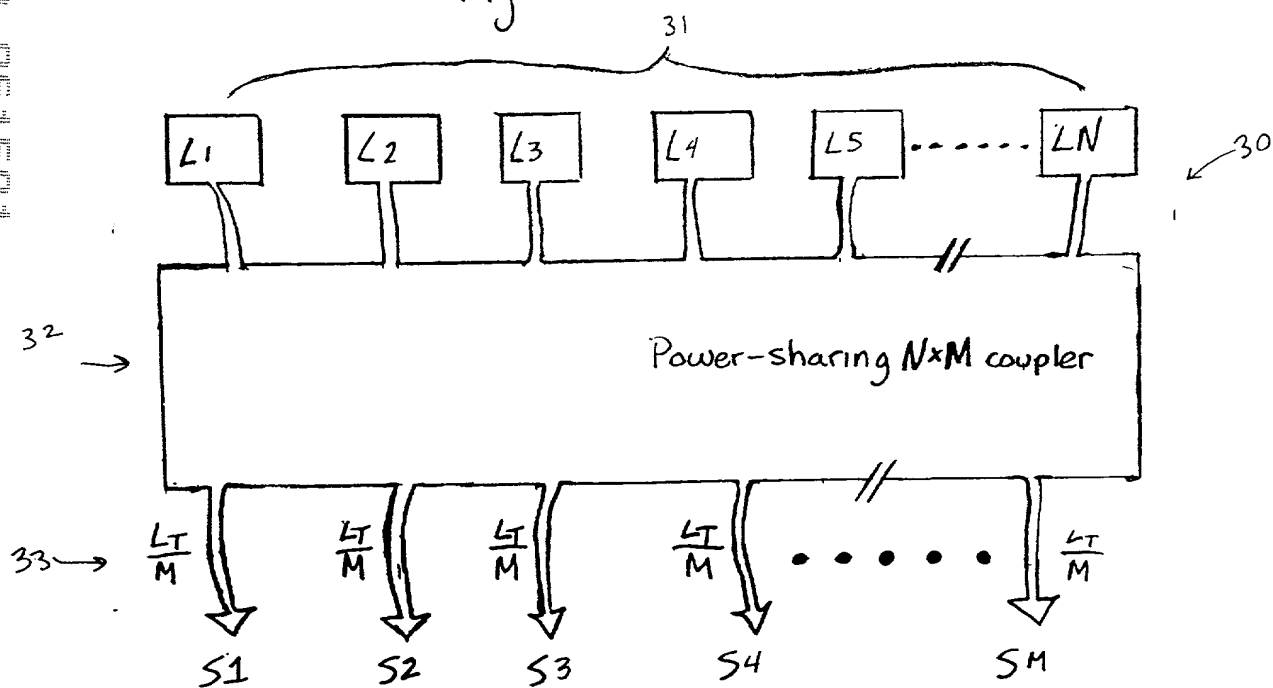


Figure 2

FIG. 3a

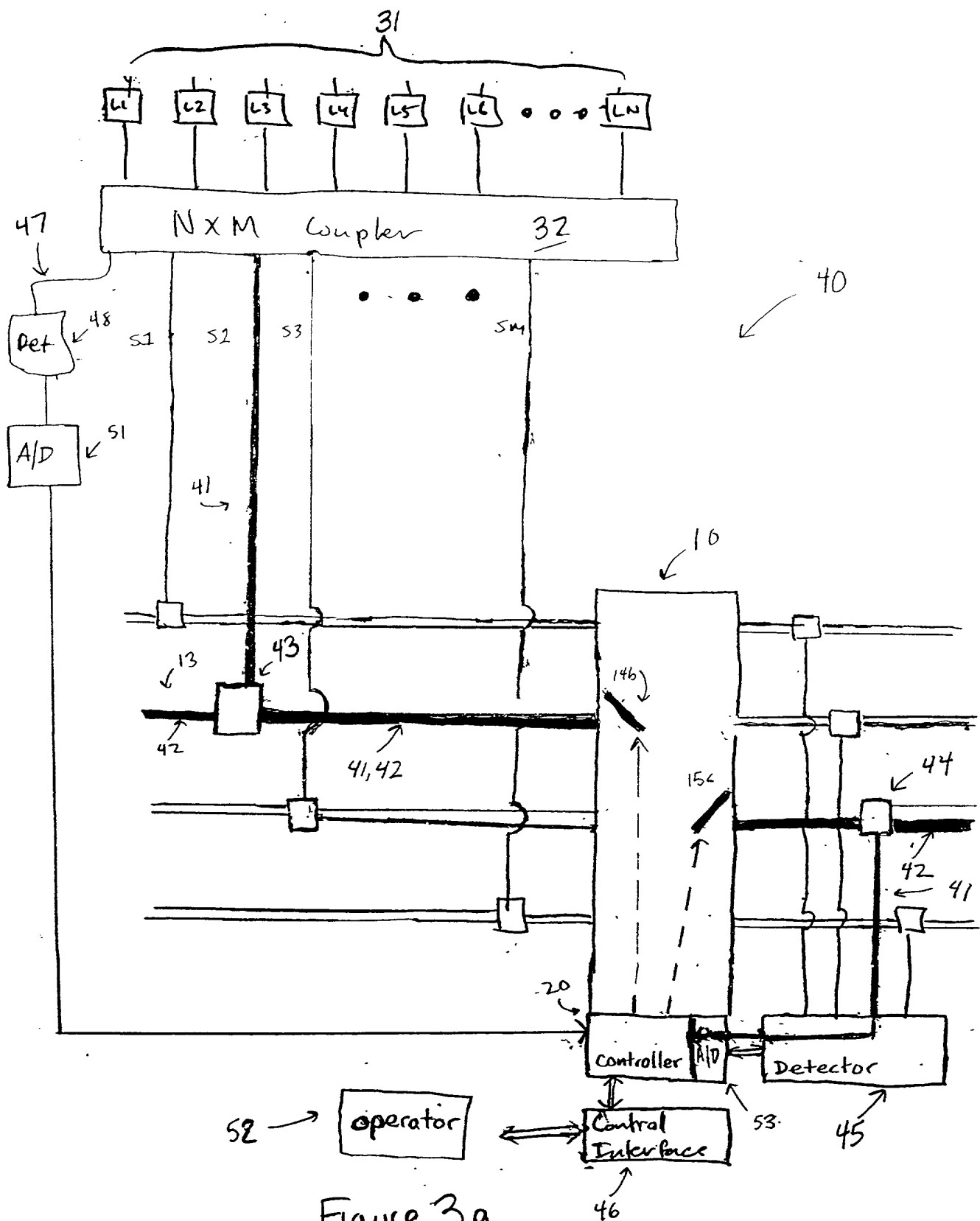


FIG. 3b is a schematic diagram of a system 10' showing a central processing unit 32a, 32b, and 32c connected to a plurality of input/output devices 31a, 31b, and 31c. The system 10' includes a central processing unit 32a, 32b, and 32c, and a plurality of input/output devices 31a, 31b, and 31c. The central processing unit 32a is connected to the input/output devices 31a and 31b. The central processing unit 32b is connected to the input/output devices 31b and 31c. The central processing unit 32c is connected to the input/output devices 31c and 31a. The input/output devices 31a, 31b, and 31c are connected to the central processing unit 32a, 32b, and 32c via a bus 33a, 33b, and 33c. The bus 33a, 33b, and 33c are connected to the input/output devices 31a, 31b, and 31c via a plurality of lines 54a, 54b, and 54c. The lines 54a, 54b, and 54c are connected to the input/output devices 31a, 31b, and 31c via a plurality of ports 54a, 54b, and 54c. The ports 54a, 54b, and 54c are connected to the input/output devices 31a, 31b, and 31c via a plurality of lines 54a, 54b, and 54c. The lines 54a, 54b, and 54c are connected to the input/output devices 31a, 31b, and 31c via a plurality of ports 54a, 54b, and 54c. The ports 54a, 54b, and 54c are connected to the input/output devices 31a, 31b, and 31c via a plurality of lines 54a, 54b, and 54c.

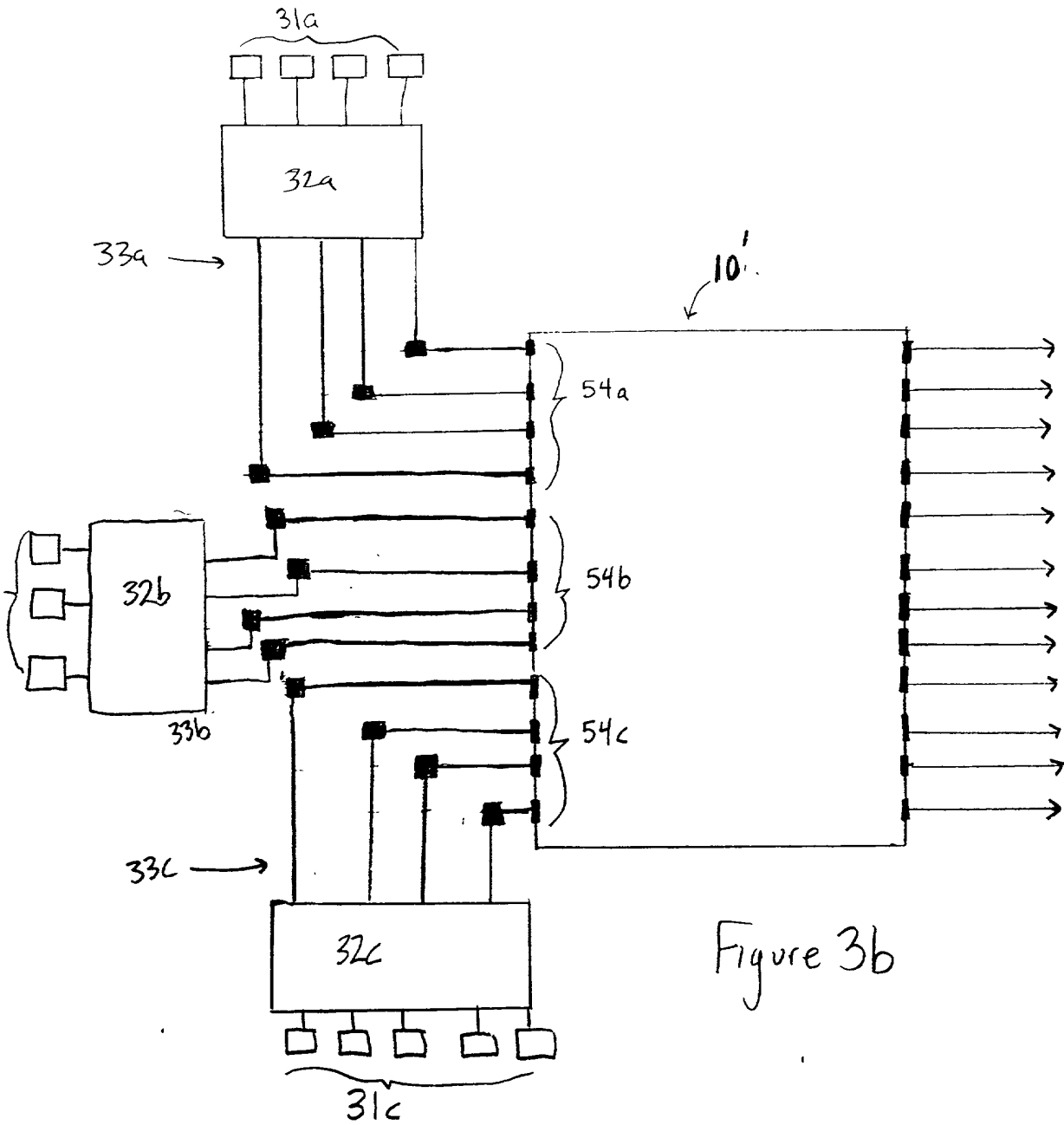


Figure 3b

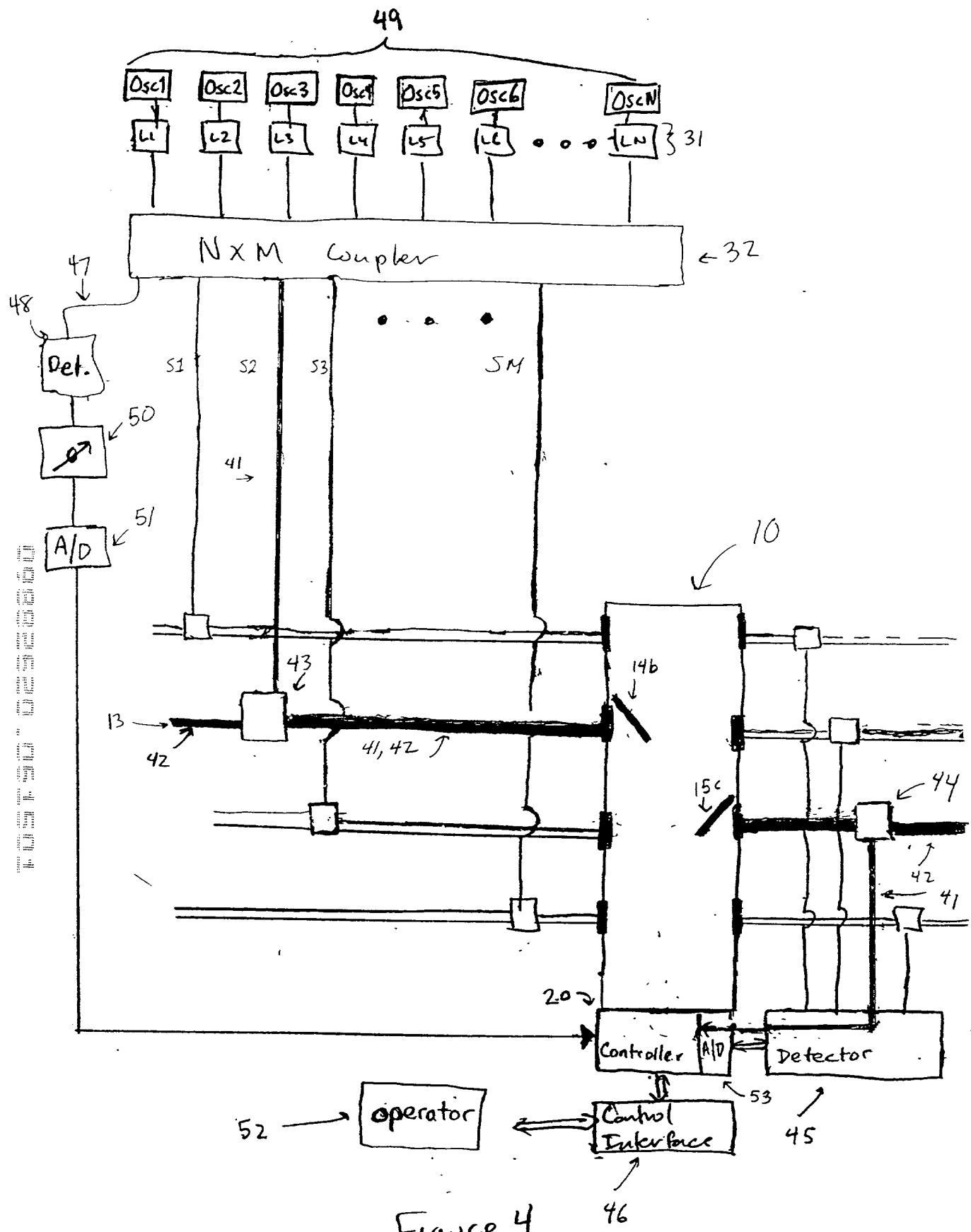


Figure 4